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|---|---|
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| **ART UNIT** | **PAPER NUMBER** |
| 2113 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/886,959 | AVIZIENIS, ALGIRDAS | |
| | Examiner | Art Unit | |
| | Bryce P. Bonzo | 2113 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24,27,33-38,41-61 and 63-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24,27,33-38,41-61 and 63-83* is/are rejected.

7)☒ Claim(s) *84* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

# NON-FINAL OFFICIAL ACTION

## *Status of the Claims*

Claim 79 is rejected under 35 USC §112, first paragraph.

Claims 2, 3, 7, 12, 19, 24, 27, 41, 54, 61, 64 and 65-69 are rejected under 35 USC §112, second paragraph.

Claims 4, 16, 36, 47, 59, 63, 66 and 82 are rejected under 35 USC §112, fourth paragraph.

Claims 1, 4-9, 11, 13-17, 19-21, 42-45, 47, 48, 53, 54, 63, 70, 76, 77 and 79 are rejected under 35 USC §102(b).

Claims 2, 3, 10, 12, 18, 22-24, 33-38, 41, 46, 49, 50, 51, 52, 55-61, 64-69, 71-75, 78 and 80-83 are rejected under 35 USC §103.

Claim 84 is objected to while containing allowable subject matter.

## *Rejections under 35 USC §112, first paragraph*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 79 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one

skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. At not point in the specification is it ever discussed whether the claimed invention is a circuit breaker. This claim is believed to be a result of a conversation with Applicant, and as such was not held by Applicant at the time of the filing of the disclosure.

***Rejections under 35 USC §112, second paragraph***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2, 3, 7, 12, 19, 24, 27, 41, 54, 61, 64 and 65-69 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 2, 3, 7, 12, 19, 24, 27, 41, 54, 61, 64 and 65-69, the Examiner is unable to determine the bounds of "substantially exclusively made up of substantially commercial, off-the-shelf components." The Examiner is unable to determine a reasonable limit to the claims. Applicant responses to this rejection previously reaffirm the Examiner's inability to precisely define metes and bounds of the claims.

***Rejections under 35 USC §112, fourth paragraph***

The following is a quotation of the fourth paragraph of 35 U.S.C. 112:

> Subject to the following paragraph, a claim in dependent form shall contain a reference to a claim previously set forth and then specify a further limitation of the subject matter claimed. A claim in dependent form shall be construed to incorporate by reference all the limitations of the claim to which it refers.

Claims 4, 16, 36, 47, 59, 63, 66 and 82 are rejected under 35 USC §112, fourth paragraph as they fail to further limit the scope of the claims. The *such computer system* of these claims is each case has already been claimed verbatim in the parent claim. These claims recite a "such computer." Each claim depends from a parent claim containing in the preamble: "failure of a computer system." Each parent claim then recites the failure in the body of the claim. As the failure is recited in the body of the claim, the descriptors from the preamble breath life into the bodily recited limitation and warrant patentable weight. As the Examiner is then required to find the computer system, reciting "such computer system" in its own claim becomes a redundant limitation, and when presented singularly fails to meet the requirements of §112, fourth paragraph, namely that a dependant claim must further limit the parent. Additionally, the preamble of the claims set forth the claiming of the apparatus used with the computer not, the computer system for which it is used.

***Rejections under 35 USC §102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4-9, 11, 13-17, 19-21, 42-45, 47, 48, 53, 54, 63, 70, 76, 77 and 79 rejected under 35 U.S.C. 102(b) as being anticipated by Best (United Stats Patent No. 4,99,5,040).

Best discloses:

1. Apparatus for deterring failure of a computing system; said apparatus comprising:

a hardware network of components, having substantially no software and substantially no firmware except programs held in an unalterable read-only memory (Figures 3, 4 and 5 disclose a hardware network of fault detection and handling components);

terminals of the network for connection to such system (Figure 4, message channel and associated buffers act as terminals, column 3, lines 8-15);

fabrication-pre-programmed hardware circuits of the network for guarding such system from failure (column 6, lines 23-27).

4. The apparatus of claim 1, further comprising:

such computing system (column 3, lines 2-7).

5. The apparatus of claim 1, wherein:

the circuits comprise portions for identifying failure of the any of the circuits and correcting for the identified failure (column 6, lines 10-14).

6. The apparatus of claim 1, wherein:

the circuits are not operable of running an application program (column 6, lines 28-45: no application programs are disclosed and the logic elements are simple comparators and voters which the capability to carry out application execution).

7. The apparatus of claim 1, particularly for use with a computing system that is substantially exclusively made of commercial off the shelf components and that has at least one hardware component for generating a response of the system to failure (column 6, lines 10-14 the computer system will generate abnormal/incorrect data and place it onto the bus); and wherein:

the circuits comprise portions for reacting to said response of such hardware subsystem (column 6, lines 10-14).

8. The apparatus of claim 1, particularly for use with a computing system that has plural generally parallel computing channels (column 5, lines 26-59); and wherein:

the circuits comprise portions for comparing computational results from such parallel channels (column 5, lines 26-59).

9. The apparatus of claim 8, wherein:

the parallel channels of such computing system are of diverse design or origin (column 3, lines 5: the channels are attached to different computer systems and thus are generated at a diverse origin).

11. The apparatus of claim 1, wherein:

the circuits comprise modules for collecting and responding to data received from at least one of the terminals (column 5, lines 26-39), said modules comprising:

at least there data collecting and responding modules (column 5, lines 26-39), and

processing sections for conferring among the modules to determine whether any of the modules has failed (column 5, lines 43-59).

79. The apparatus of claim 1, wherein:

the apparatus is not a circuit breaker (Fig 3 does not incorporate a circuit breaker).

13. Apparatus for deterring failure of an entire computing system, wherein the computing system optionally includes plural mutually redundant modules; said apparatus comprising:

a network of components having terminals for connection to such system, wherein the network is constructed to be initially and permanently distinct from such computing system including all of such redundant modules (Figures 3, 4, and 5 show the voting and recovery circuitry being separate from the plural data channels coming off of the redundant processors inherent to the computer not shown);

circuit of the network for operating programs to guard such entire systems from failure (column 6, lines 23-27);

the circuits comprising portions for identifying failure of any of the circuits and correcting for the identified failure (column 6, lines 2).

14. The apparatus of claim 13, wherein:

the program-operating portions comprise a section that corrects for the identified failure by automatically taking a failed circuit out of operation (column 6, lines 10-14).

15. The apparatus of claim 13, wherein:

the network is an infrastructure that continuously waits to respond to messages from such system (columns 3 and 4 show an apparatus which uses comparators to check messages continuously).

16. The apparatus of claim 16, further comprising:

such computing system (column 4, lines 1-25).

21. The apparatus of claim 16, wherein:

the computer system has parallel channels that are of diverse deign or origin (column 3, lines 5: the channels are attached to different computer systems and thus are generated at a diverse origin).

17. The apparatus of claim 13, wherein:

the program-operating portions comprise at least three of the circuits (column 3-14 and Figure 4); and

failure is identified at least in part by majority vote among the at least three circuits (column 5, lines 43-51).

19. The apparatus of claim 13, particularly for use with a computing system that is substantially exclusively made of commercial, off-the-shelf components and that has at least one hardware subsystem for generating a response of the system to failure (column 6, lines 10-14); and wherein:

the circuits comprise portions for reacting to said response of such hardware subsystems (column 6, lines 10-14).

20. The apparatus of claim 13, particularly for use with a computing system that has plural generally computing channels (column 5, lines 26-35); and wherein:

the circuits comprise portions for comparing computational results from such parallel channels (column 5, lines 43-51).

70. The apparatus of claim 13, wherein:

the circuits do not and cannot operate any application program (column 6, lines 28-45: no application programs are disclosed and the logic elements are simple comparators and voters which the capability to carry out application execution).

42. Apparatus for deterring failure of an entire computing system that is distinct from the apparatus and that has plural generally parallel computing channels and has at least one application input module and at least one processor for running an application program; said apparatus comprising:

a network of components having terminals for connection to such system (Figures 3, 4 and 5); and

circuits of the network for operating programs to guard such entire system from failure wherein the network is constructed to be initially and permanently distinct from such computing system (Figures 3, 4 and 5 show a clear delineation between the plural processing channels of the computer system which feed into message buffers and fault detecting and handling system which protects it) (a) every such application-data input module (the protection buffers receive the data from these elements and thus can not be them) and (b) every such application-program processor (the computer disclosed as running the applications are not part of the protection system, but are at the other end of a bus), and (c) all of such parallel computing channels (Figures3-5 clearly show the

computer channels feeding into a separate buffering system separates the protection system from the computer system);

the circuits comprising portions for comparing computational results from such parallel channels (column 5, lines 26-29).

47. The apparatus of claim 42, further comprising:

such computer system (column 4, lines 1-13).

43. The apparatus of claim 47, wherein:

the parallel channels of the computing system are of diverse design or origin (column 3, lines 5: the channels are attached to different computer systems and thus are generated at a diverse origin).

44. The apparatus of claim 42, wherein:

the comparing portions comprise at least one section for analyzing discrepancies between the results from such parallel channels (column 5, lines 26-59).

48. The apparatus of claim 42, wherein:

the circuits do not and cannot operate any application program (column 6, lines 28-45: no application programs are disclosed and the logic elements are simple comparators and voters which the capability to carry out application execution).

53. The apparatus of claim 42, wherein:

the circuits comprise modules for collecting and responding to data received from at least one of the terminals (column 5, lines 26-39), said modules comprising:

at least three data-collecting and responding modules (column 5, lines 26-39), and

processing sections for conferring among the modules to determine whether any of the modules has failed (column 5, lines 43-59).

62. Apparatus for deterring failure of an entire computer system that is distinct from the apparatus and has at least one application data input module, and at least one processor for running an application program; said apparatus comprising:

a network of components having terminals for connection to such system (Figures 3-5); and

circuits of the network for operating programs to guard such entire system from failure (column 6, lines 23-67);

the circuits comprising modules for collecting and responding to data received from at least one of the terminals (column 5, lines 26-39), said modules comprising:

at least three data-collecting and –responding modules (column 5, lines 26-39), and

processing sections for conferring among the modules to determine whether any of the modules has failed (column 5, lines 43-59);

wherein the network, including all of the modules and sub-modules substantially (Figures 3, 4 and 5 show a clear delineation between the plural processing channels of the computer system which feed into message buffers and fault detecting and handling system which protects it) (a) every such application-data input module (the protection buffers receive the data from these elements and thus can not be them) and (b) every such application-program processor (the computer disclosed as running the applications are not part of the protection system, but are at the other end of a bus), and (c) all of processing sections (Figures3-5 clearly show the computer channels feeding into a separate buffering system separates the protection system from the computer system) is constructed to be initially and permanently distinct from such computing system.

63. The apparatus of claim 62, further comprising:

such computing system (column 4, lines 1-25).

76. The apparatus of claim 62, wherein:

the circuits cannot and do not run any application program (column 6, lines 28-45: no application programs are disclosed and the logic elements are simple comparators and voters which the capability to carry out application execution).

77. The apparatus of claim 62, wherein:

the circuits protect the entire such system (column 3, lines 21-28).

***Rejection under 35 USC §103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 10, 12, 18, 22-24, 33-38, 41, 46, 49, 50, 51, 52, 55-61, 64-69, 71-75, 78 and 80-83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Best (United States Patent No. 4,995,040) in view of Avižienis (*The N-Version Approach to Fault-Tolerant Software*, 1985, it is further acknowledged, that Dr. Avižienis is the current named inventor of the present application).

2. Best does not disclose, while Avižienis teaches:

at least one of the network terminals is connected to receive one error signal generated by such system in event of incipient failure of such a system (page 1498 describes how the Decision and Executive layer receives exceptions from the version layer indicating errors within the instance running that particular version of the software);

at least one of the network terminals is connected to provide one recovery signal to such system upon receipt of the error signal (page 1498 describe the use of the local executive processing faults and providing and solution to the problem); and

the apparatus further comprises means for automatically responding to the at least one error signal by generating the at least one recovery signal for guarding all

such system against failure (page 1498 discloses the local and global executives at differing levels providing commands to the version which prevent failure).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

3. Best does not disclose, while Avižienis teaches:

the network is an interface which is generic in that it can accommodate any such system that can issue an error message and handle recovery command (page 1498: DEDIX hides all the fault processing from the version layer, and it is the decision and executive layer which performs this functionality, making it generic).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of

avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

10. Best does not disclose, while Avižienis teaches:

particularly for use with a computer system that has plural processors (Best does disclose use with "dissimilar computing elements for performing computing operations" but not specifically processors; Avižienis does disclose processor indirectly by monitoring for processor errors on page 1498: "dependent on a specific computer system...implementation technique"); and wherein:

the circuits comprise portions for identifying failure of any such processors and correcting for identified failure (page 1498 discloses how Avižienis handles processor faults, while Best simply handles any fault coming down the communication channel).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into

separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

12. Best does not disclose, while Avižienis teaches:

particularly for use with a computing system that is substantially exclusively made of commercial, off-the-self components and that has at least one subsystem for generating a response to failure (page 1498 describes the Version layer reporting errors and receiving decisions results).

the circuits comprise portions for interposing analysis and a corrective action between the response-generating subsystem and the command receiving subsystem (page 1498 describes the Version layer reporting errors and receiving decisions results

and those result come from the decision and executive layer; Best further describes interposing circuitry for detection and correction at column 5, lines 43-51).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

80. Best does not disclose, while Avižienis teaches:

at least one of the network terminals is connected to receive at least one error signal generated by such system in event of incipient failure (page 1498 discloses specific application and OS error messages handled by the Local executive, Best discloses detecting the failures itself from the data on the channel);

at least one of the network terminals is connected to provide at least one recovery signal to such system upon receipt of the error signal (page 1498 discloses specific application and OS error recovery commands handled by the Local executive, while Best discloses substituting the correct data onto the channel).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes,

and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

18. Best does not disclose, while Avižienis teaches:

said circuits receive from such system error messages warning of incipient failure, and issue recovery commands to such system (page 1498 discloses specific application and OS error recovery commands handled by the Local executive, while Best discloses substituting the correct data onto the channel).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into

separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

22. Best does not disclose, while Avižienis teaches:

particularly for use with a computing system that has plural processors (Best does disclose use with "dissimilar computing elements for performing computing operations" but not specifically processors; Avižienis does disclose processor indirectly by monitoring for processor errors on page 1498: "dependent on a specific computer system...implementation technique"); and wherein:

the circuits comprise portions for identifying failure of any such processors and correcting for identified failure (page 1498 discloses how Avižienis handles processor faults, while Best simply handles any fault coming down the communication channel).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

23. Best does not disclose, while Avižienis teaches:

the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and handle recovery command (page 1498: DEDIX hides all the fault processing from the version layer, and it is the decision and executive layer which performs this functionality, making it generic).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of

Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

24. Best does not disclose, while Avižienis teaches:

particularly for use with a computing system that is substantially exclusively made of commercial, off-the-self components and that has at least one subsystem for generating a response to failure , and that also has at least one subsystem for receiving recovery commands (page 1498 describes the Version layer reporting errors and receiving decisions results).

the circuits comprise portions for interposing analysis and a corrective action between the response-generating subsystem and the command receiving subsystem (page 1498 describes the Version layer reporting errors and receiving decisions results and those result come from the decision and executive layer; Best further describes interposing circuitry for detection and correction at column 5, lines 43-51).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into

separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

33. Best discloses:

Apparatus for deterring failure of a computing system:

a network of components having terminals for connection to such system ( Figure 3-5); and

circuits of the network for operating programs to guard such system from failure (column 6, lines 23-27).

Best does not explicitly disclose, while Avižienis teaches:

Apparatus that is substantially exclusively made of commercial, off-the-shelf components and that has at least one hardware subsystem for generating an error message of the system about incipient failure (page 1498 describes the Version layer reporting errors and receiving decisions results),

the portions for reacting to such error message of such hardware system (1498 discloses the Local and global executives performing these functions).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray

and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

34. Best discloses:

the circuits guard the entire such system from failure (column 3, lines 21-27).

35. Best does not disclose, while Avižienis teaches:

the network is an interface which is generic in that it can accommodate any such system that can issue an error message and handle recovery command (page 1498: DEDIX hides all the fault processing from the version layer, and it is the decision and executive layer which performs this functionality, making it generic).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column

2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

36. Best in combination with Avižienis teaches:

such computing system, including such hardware system. (column 3, lines 21-29).

37. Best discloses:

the computing system has plural generally parallel computing channels(column 5, lines 26-59); and

the parallel channels of the computing system are of diverse design or origin (column 5, lines 26-59).

38. Best discloses:

said circuits are not operable of running an application program (column 6, lines 28-45: no application programs are disclosed and the logic elements are simple comparators and voters which the capability to carry out application execution).

41. Best does not explicitly disclose, while Avižienis teaches:

particularly for use with a computing system that is substantially exclusively made of commercial, off-the-self components and that has at least one subsystem for generating a response to failure , and that also has at least one subsystem for receiving recovery commands (page 1498 describes the Version layer reporting errors and receiving decisions results).

the circuits comprise portions for interposing analysis and a corrective action between the response-generating subsystem and the command receiving subsystem (page 1498 describes the Version layer reporting errors and receiving decisions results and those result come from the decision and executive layer; Best further describes interposing circuitry for detection and correction at column 5, lines 43-51).

46. Best does not explicitly disclose, while Avižienis teaches:

the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and handle recovery command (page 1498: DEDIX hides all the fault processing from the version layer, and it is the decision and executive layer which performs this functionality, making it generic).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the

time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

49. Best does not disclose, while Avižienis teaches:

said circuits receive from such computing system error messages warning of incipient failure, and issue recovery commands to such system (page 1498 discloses specific application and OS error recovery commands handled by the Local executive, while Best discloses substituting the correct data onto the channel).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear

intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

52. Best does not disclose, while Avižienis teaches:

particularly for use with a computing system that has plural processors (Best does disclose use with "dissimilar computing elements for performing computing operations" but not specifically processors; Avižienis does disclose processor indirectly by monitoring for processor errors on page 1498: "dependent on a specific computer system... implementation technique"); and wherein:

the circuits comprise portions for identifying failure of any such processors and correcting for identified failure (page 1498 discloses how Avižienis handles processor faults, while Best simply handles any fault coming down the communication channel).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed

data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

54. Best does not disclose, while Avižienis teaches:

particularly for use with a computing system that is substantially exclusively made of commercial, off-the-self components and that has at least one subsystem for generating a response to failure (page 1498 describes the Version layer reporting errors and receiving decisions results).

the circuits comprise portions for interposing analysis and a corrective action between the response-generating subsystem and the command receiving subsystem (page 1498 describes the Version layer reporting errors and receiving decisions results and those result come from the decision and executive layer; Best further describes interposing circuitry for detection and correction at column 5, lines 43-51).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the

time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

50. Best discloses:

Apparatus for deterring failure of a computing system that is distinct from the apparatus and that has plural generally parallel computing channels; said apparatus comprising:

a network of components having terminals for connection to such system (Figures 3-5); and

circuits of the network for operating programs to guard such system from failure, wherein such network is constructed to initially distinct from such computing system including all of such plural computing channels (Figures 3-5);

the circuits comprising portions for comparing computational results from such parallel channels (Figures 3-5).

Avižienis teaches:

the comparing means portions comprise circuitry for performing an algorithm to validate a match that is inexact (page 1498); and

the algorithm-performing circuitry employs a degree of inexactness suited to a type of computation under comparison (page 1498).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

51. Best in combination with Avižienis discloses:

the algorithm-performing circuitry performs an algorithm that selects a degree of inexactness based on the type of computation under comparison (page 1498); and

the circuits also impose corrective action upon such system based upon discrepancies found by the comparing portion (column 6, lines 10-14).

71. Best discloses:

the circuits do not and cannot operate any application program (column 6, lines 28-45: no application programs are disclosed and the logic elements are simple comparators and voters which the capability to carry out application execution).

72. Best discloses:

the circuits protect the entire such system (column 3, lines 21-27).

73. Best does not disclose, while Avižienis teaches:

said circuits receive from such system error messages warning of incipient failure, and issue recovery commands to such system (page 1498 discloses specific application and OS error recovery commands handled by the Local executive, while Best discloses substituting the correct data onto the channel).

74. Best does not disclose, while Avižienis teaches:

the network is an infrastructure which is generic in that it can accommodate any such system that can issue an error message and handle recovery command (page

1498: DEDIX hides all the fault processing from the version layer, and it is the decision and executive layer which performs this functionality, making it generic).

55. Best discloses:

Apparatus for deterring failure of any computer system, said apparatus comprising:

a network of components having terminals for connection to such system, wherein the network is constructed to be initially and permanently distinct from such computing system including all of such redundant modules (Figures 3, 4, and 5 show the voting and recovery circuitry being separate from the plural data channels coming off of the redundant processors inherent to the computer not shown);

circuit of the network for operating programs to guard such entire systems from failure (column 6, lines 23-27);

the circuits comprising portions for identifying failure of any of the circuits and correcting for the identified failure (column 6, lines 2).

Best does not disclose while, Avižienis teaches:

system that has plural processors (Best does disclose use with "dissimilar computing elements for performing computing operations" but not specifically processors; Avižienis does disclose processor indirectly by monitoring for processor errors on page 1498: "dependent on a specific computer system...implementation technique") and is capable of generating error messages warning of incipient failure,

and capable of responding to recovery command (page 1498 discloses specific application and OS error recovery commands handled by the Local executive, while Best discloses substituting the correct data onto the channel).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of

Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

75. Best discloses:

the program-operating circuits guard any such system from failure by issuing a recovery command (column 6, lines 10-14).

Avižienis discloses:

the failure-identifying and correcting portion provide the recovery command (page 1498).

56. Avižienis discloses:

the identifying portions comprise a section that corrects for the identified failure by taking the failed processor out of operations (page 1498).

57. Best discloses:

the circuits cannot and do not run an application program (column 6, lines 28-45: no application programs are disclosed and the logic elements are simple comparators and voters which the capability to carry out application execution).

58. Best discloses:

the circuits protect the entire such system (column 3, lines 21-28).

59. Best discloses:

such computing system (Figure 1).

61. Best and Avižienis disclose:

the circuits comprise portions for interposing analysis and a corrective action between the response-generating subsystem and the command receiving subsystem (page 1498 describes the Version layer reporting errors and receiving decisions results and those result come from the decision and executive layer; Best further describes interposing circuitry for detection and correction at column 5, lines 43-51).

Avižienis discloses:

particularly for use with a computing system that is substantially exclusively made of commercial, off-the-self components and that has at least one subsystem for generating a response to failure (page 1498 describes the Version layer reporting errors and receiving decisions results).

64. Best in combination with Avižienis discloses:

particularly for use with a computing system that is substantially exclusively made of commercial, off-the-self components and that has at least one subsystem for generating a response to failure, and that also has at least one subsystem for receiving recovery commands (page 1498 describes the Version layer reporting errors and receiving decisions results).

the circuits comprise portions for interposing analysis and a corrective action between the response-generating subsystem and the command receiving subsystem (page 1498 describes the Version layer reporting errors and receiving decisions results and those result come from the decision and executive layer; Best further describes interposing circuitry for detection and correction at column 5, lines 43-51).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the

time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

73. Best does not disclose, while Avižienis teaches:

said circuits receive from such system error messages warning of incipient failure, and issue recovery commands to such system (page 1498 discloses specific application and OS error recovery commands handled by the Local executive, while Best discloses substituting the correct data onto the channel).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear

intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

65. Best discloses:

circuits of the network for operating programs to guard such system failure (column 5, lines 23-27);

the circuits comprising portions for interposing analysis and corrective action between the response-generating subsystem and the command-receiving subsystem (column 5, lines 43-51),.

Avižienis discloses:

Apparatus for deterring failure of a computing system that is substantially exclusively made of commercial, off the shelf components and that has at least one subsystem for generating a response of the system to failure, and that also has at least one subsystem receiving recovery commands (page 1498 describes the Version layer reporting errors and receiving decisions results), ; said apparatus comprising:

a network of components having terminals for connection to such system between the response-generating subsystem and the recovery-command-receiving subsystem (Figure 2).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of

Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

66. Best discloses:

such computing system (column 5, lines 23-27).

67. Best discloses:

the circuits cannot and do not run any application programs (column 6, lines 28-45: no application programs are disclosed and the logic elements are simple comparators and voters which the capability to carry out application execution).

68. Best discloses:

the circuits protect the entire such system (column 3, lines 21-28).

69. Best does not disclose, while Avižienis teaches:

the network is an interface which is generic in that it can accommodate any such system that can issue an error message and handle recovery command (page 1498: DEDIX hides all the fault processing from the version layer, and it is the decision and executive layer which performs this functionality, making it generic).

81. Avižienis discloses:

An infrastructure for a computing system that has at least one computing node (the server running the Version layer) for running at least one application program (the N Version); said infrastructure comprising:

at least one monitoring node (M-node) for monitoring the condition of the at least one C-node by waiting for an error signal, indicating incipient failure, from the at least one C-node and responding to the error signal by sending a recovery command to the at least one C-node (the Decision and Executive Layer is interpreted as the M-Node and performs these function as listed on page 1498); and

at least one adapter node (a-node) for transmitting the error signal and recovery command between the at least one C-node and at least M-node (1497, figure 2, box labeled sender performs this function) .

Avižienis does not explicitly disclose, Best teaches:

the at least one M-Node is manufactured to be and remains wholly distinct from the at least one C-node (Figure 3, column 3, lines 21-29).

the at least M-Node cannot, and does not, run any application program (Figure 3, column 6, lines 28-48 disclose only safe guard functionally being programmed).

Best as shown above discloses a hardware based system to monitor plural processing/computing channels for errors in a separate computing system (column 3, lines 15-29; column 4, lines 14-25). Best further discloses that his system is application

to all types of digital systems (column 6, lines 29-61) and further are further applicable at any level (column 6, lines 42-47). Avižienis teaches the use of the DEDIX distributed data processing system, and more importantly that is may implemented in single computer and multiple computer acting in concert across a network (page 1497, column 2). Avižienis further describes the fault handling system as being separated into separate distinct layers (page 1497, column 2). Avižienis further describes the needs as an architectural need: hardware voting and consistency checking (page 1496, column 1). From these passages one of ordinary skill concludes that Avižienis has expressed a need for a hardware support structure to manage the voting he describes, and that it can be implemented in multiple distribution styles. Best provides a clear intend to be used in hardened voting schemes with processors which may go astray and must be corrected timely (specifically avionics, which as a side note Avižienis produces later papers on the need for such system in space craft, as specialization of avionics). Therefor it would have been obvious to one of ordinary skill in the art at the time of invention to implement the fault tolerant portions of the layered DEDIX system of Avižienis with the hardware fault locating and handling system of Best, thereby creating a stronger N-Version software system.

82. Best discloses:

such computing system (column 5, lines 23-27).

83. Avižienis discloses:

a decision making node (D-node) for comparing output data generated by such plural C-nodes and reporting to the at least one M-Node any discrepancy between the output data (generic decision algorithm of page 1498); and wherein:

the at least one M-node analyzes the D-node reporting, and based thereon then arbitrates among the C-nodes (the local and global executives determine solution and carry them out).

### *Allowable Subject Matter*

Claim 84 is objected to while containing allowable subject matter. Applicant is advised this indication of allowable matter is in view of the claim as a whole and any modification to the scope of the claim may result in a Final Official Action.

### *Response to Applicant's Arguments*

As new grounds of rejections based on prior art have been given, Applicant's arguments are moot.

The record in clear on the Examiner's position with regard to the rejections under 35 USC §112.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P. Bonzo whose telephone number is (571)272-3655. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P. Bonzo

Bryce P Bonzo
Primary Examiner
Art Unit 2113